A LOW-COST VIDEO CAMERA FOR MACHINE VISION AND CONSUMER USE

Robin Bradbeer
Department of Electronic Engineering, City Polytechnic of Hong Kong
88 Tat Chee Avenue, Kowloon Tong, Hong Kong

Tel: +852 788 7199 Fax: +852 788 7791 E-mail: eertbrad@cityu.edu.hk

Abstract

There is a constant, even growing, demand for low cost, light weight, video cameras for industrial, research and consumer use. Examples of such uses include toys, security, industrial automation and robotic vision. This paper presents the first stages of development of a low cost camera, initially for toy use, with a target manufacture price of $20, but with applications in many of the areas stated above.

Introduction

The most popular method for abstracting visual information using video cameras is based around image grabbing techniques. This is expensive, bulky and quite often too slow. It also requires the use of large amounts of processing power. In its simplest form most of this effort is wasted.

Video cameras using these techniques usually use a ccd array as the image sensor. The information from that array is then converted to internationally accepted standards which is then available in a 1 Vpp analogue format. The video processing system then has to grab each frame and convert each pixel into a binary code that can be stored in memory.

In many applications the camera is in close proximity to the processing unit. Thus the conversion to analogue form is not necessary. The camera described here takes the analogue information from the ccd array, processes it through a simple A-to-D flash converter and then uses an off-the-shelf 8-bit microcontroller to process the timing signals. To achieve a 1 Vpp analogue signal, if required, a D-to-A converter can be used.

Although this is not too different from accepted techniques used in most commercially available camcorders, these have usually been designed to give near broadcast quality pictures, and in colour. For many applications low quality monochrome is all that is needed.

The main criteria for the camera described was its manufactured cost - below $20. It had to be easily mass produced and small enough to fit into mobile toys, such as radio controlled cars. It also had to have good enough resolution so it could be used in a number of machine vision applications for mobile robots and industrial automation.

Taking into account the basic design criteria it was decided to use as many standard off-the-shelf components as possible. This would allow easy manufacture of a single-chip version using design automation techniques where many embedded sub-system designs are available.

At the same time it would allow easy prototyping and testing. The design also had to be video format independent, as well as having variable scan rate and pixel resolution.

General Description of Electronics

Fig. 1 shows the general block diagram of the camera. It was decided to use an ‘off-the-shelf’ ccd array. The TC211 array from Texas Instruments is configured as a 165 by 192 pixel array. The output from the array is passed to an analogue to digital converter, which converts the analogue levels from the ccd array into digital information which is the stored in RAM.

There are two sets of memories. One is used to store the picture information from the ADC, while the other provides data to the DAC. Their positions are changed after each ‘page’, so as to maintain data output during the two read write cycles. Data is switched between the two memories using a multiplexer switching circuit (MUX). The memory control unit (MMU) initialises each cycle as well as holding the memory addresses for the data.

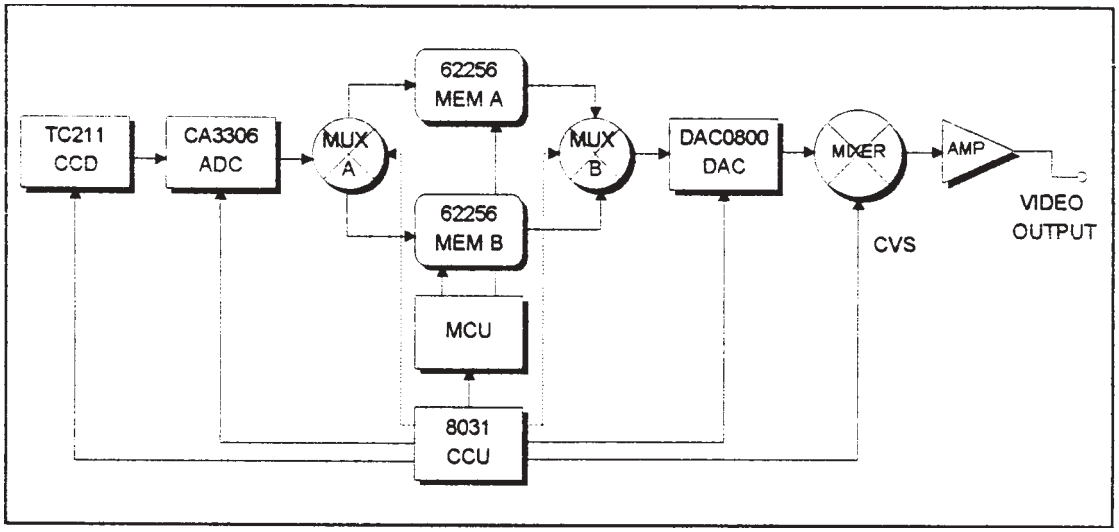

Fig. 1 The block diagram of the camera

The central control unit (CCU) provides all the handshaking signals for the ccd array, ADC, DAC and MMU. The digital to analogue converter (DAC) converts the data from the memory back into analogue form, where it is mixed with the complex sync signal generated by the CCU. This composite video signal is then fed to an amplifier to give the 1V pp standard video signal.

CCD Array

The TC211 is a full-frame charge-coupled-device image sensor, configured into 165 horizontal lines, each containing 195 pixels - Fig 2. Twelve additional pixels are provided at the end of each line to establish a dark reference and the line clamp. The antiblooming feature is activated by support clock pulses to the antiblooming gate. The charge is converted to a signal voltage of 4mV per electron. The signal is further buffered by a low noise two stage source follower amplifier to provide high output drive capability.

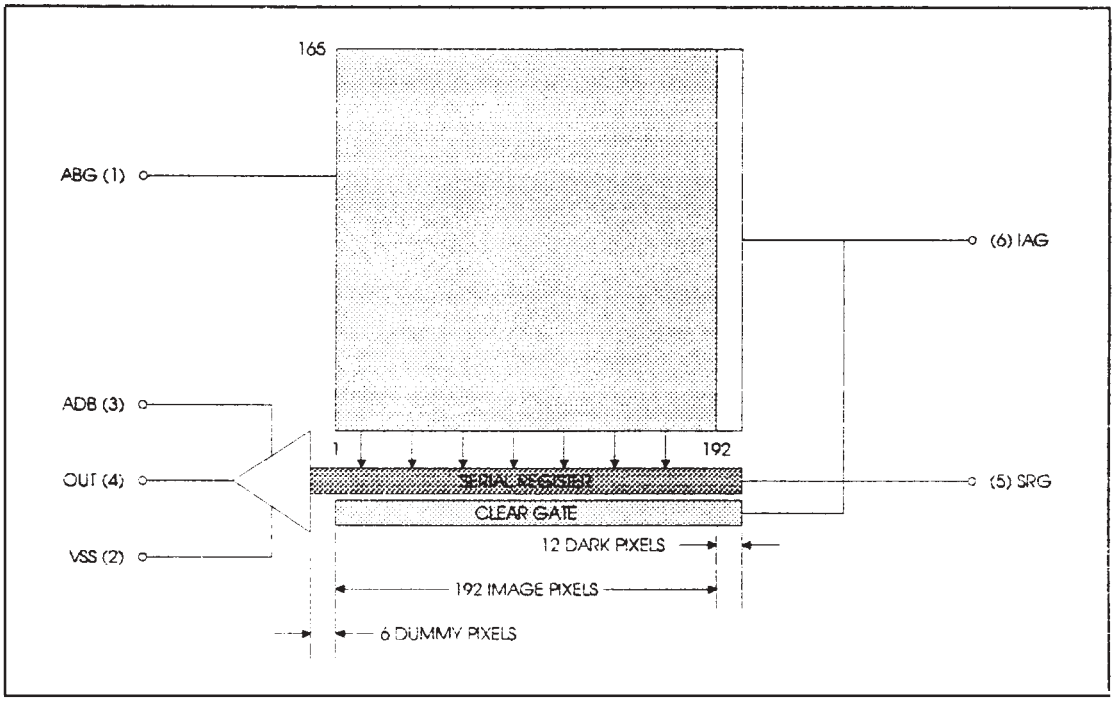

Fig 2. Functional block diagram of TC211

Each clock pulse to the image area gate causes an automatic fast clear of the 192 image pixels and 12 dark pixels of the serial register before the next image line is transferred into the serial gate. The automatic fast clear features can be used to initialise the image area by transferring all 165 image lines to the serial register under dark conditions without clocking the serial register.

The output from the ccd array is then converted to ttl levels. In the original prototype the various voltage levels required by the ccd array were generated by complex analogue circuitry. This has recently been replaced by specialised integrated circuits by TI.

Other circuit elements

Because of the speed needed to convert the signal from the array a flash ADC was used. Experimentation with the acceptable resolution of the final picture, as well as the number of grey scales required, indicated that a 6 bit ADC was necessary. The RCA-CA3306, a CMOS parallel (flash) 6 bit ADC, has a clock speed of up to 10MHz, which was adequate for this application.

The function of the switch is to control the data flow between memory and ADC, and memory and DAC. Since the data from the ADC to memory, the writing process, and the data from the memory to DAC, the reading process, take place at the same time, the circuit is used to switch the channel for the data flow. The switch was constructed from two multiplexers, one analogue, the other digital.

A high speed 8 bit current output DAC, the DAC0800, was used to convert the data. This has a conversion speed of 10MHz. As the digital signal had only 6 bits, the spare two were used to provide reference negative and positive DC bias voltages.

The signal from the DAC, as well as the complex video sync signal generated by the microprocessor, were then mixed. This was kept very simple - a single 2N3904 transistor - as the input signals had a Vpp of around 5V, whilst the output had a Vpp of 1V.

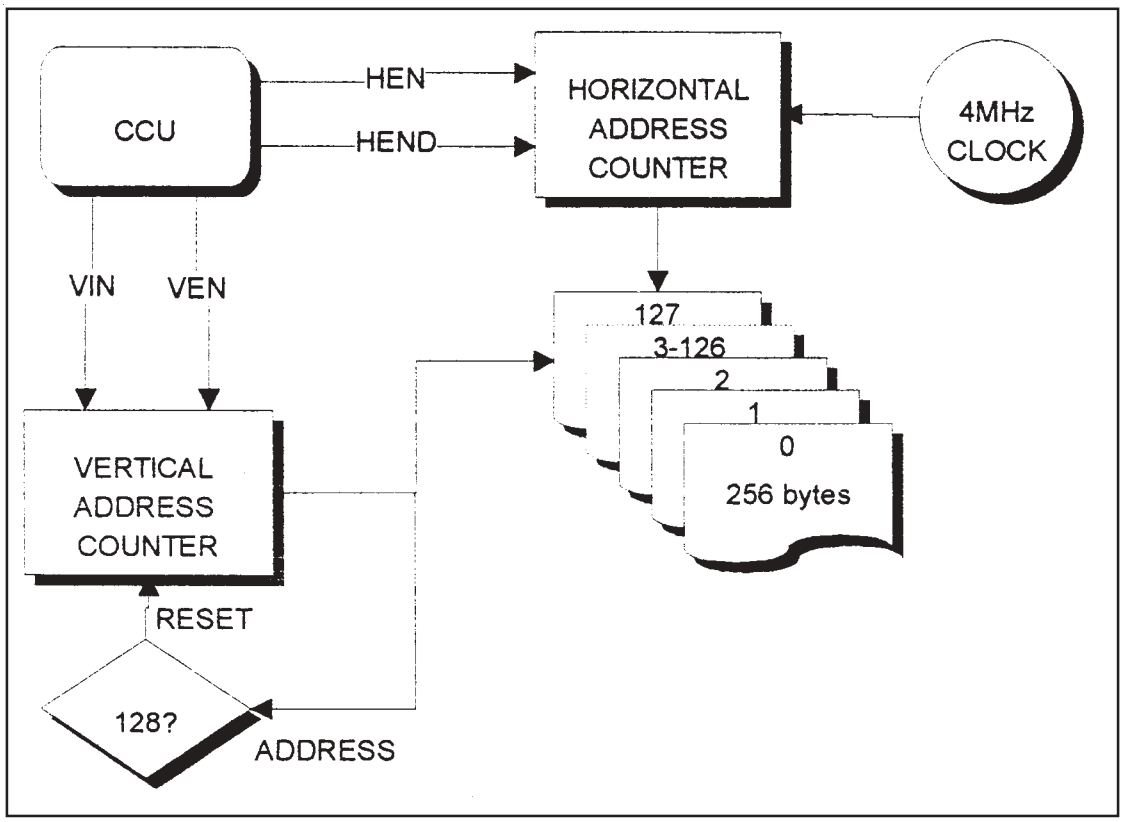

Fig 3. The block diagram of the MCU

As the speed for accessing the memory is high, 4MHz, it was not possible to generate the addresses by the micro-controller as the controller needed would be very expensive. Therefore it was necessary to construct a dedicated address counter. In fact, two counters were used, one each for the vertical and horizontal addresses. The block diagram of the memory control unit is shown in Fig 3.

An 8031 microcontroller was used as the central control unit. As this does not have internal memory and external EPROM was required.

Software

The main function of the central control unit is to generate the control signal for the components such as CCD and DAC. But the most important role is the generation of the complex video sync signal (CVS). Since the timing of the CVS is very important - it will directly affect the signal displayed on the television, the video syncs were generated before the control signals. There are two kinds of sync signal, line sync and field sync. At the same time, the camera was designed to operate using PAL or NTSC formats. As no colour information was required, the only criteria was to make sure that the sync signals could be generated under program control to give both signals.

The timing datum for the composite signal is the leading edge of the line sync pulse. This leading edge, when differentiated, produces a short pulse which is used to control the start of flyback in the television's line scan generator. This edge is preceded by a short signal to return to black level, so as not to upset the timing of the line flyback. This is known as the front porch. It is important that line flyback occurs at precisely the same point on each line if the resulting picture is not to have a ragged left edge. The front edge porch ensures that this happens whatever video information occurs at the end of the previous line.

After the line sync pulse is a longer section without video which is called the back porch. This allows extra time for the line flyback to be completed, and ensured that the electron beam is blanked throughout this period.

There is a sight difference in the line sync between NTSC and PAL video formats. But the structure of the line sync is the same, only the time duration for the major parts, such as front porch and line period. Normal televisions provide some flexibility in the timing, so some compromises can be made without causing too many problems.

The overall designed timing and the original timing for both NTSC and PAL is shown Table 1. The designed timing is rounded off to 1 μ second, since that was the smallest time that the 8031 could generate.

Horizontal Timing (ms)	NTSC	NTSC (gen)	PAL	PAL (gen)
Line period (H)	63.55	64.00	64.00	64.00
Blanking width	10.9	12.0	12.0	12.0
Sync width	4.7	5.0	4.7	5.0
Front porch	1.2	2.0	1.2	2.0
Back porch	5.0	5.0	6.1	5.0

'gen' indicates the timing generated by central control unit.

Table 1: The horizontal timing of different

From Table 1, it can be seen that the generated timing for both NTSC and PAL video formats were the same so only one line sync signal was required. In practice it was found that this caused no major problems.

For the field sync the vertical blanking interval occurs at the beginning of each field to turn off the reproducing spot while it retraces from the bottom of the picture back to the top to begin scanning of next field. For NTSC, a total of 20 horizontal scan lines are allowed for the vertical retrace interval. The vertical blanking pulse exists for this interval. The vertical sweep oscillator is controlled by the vertical sync pulses. A vertical sync pulse occurs at the

end of each field along with the vertical blanking pulse. A vertical sync pulse has a width equal to three times the horizontal. The vertical sync pulse has five serrations inserted at intervals of H/2 seconds. These serrations assure horizontal synchronisation during the vertical sync pulse.

The vertical sync pulse is immediately preceded and followed by portions of the vertical blanking interval equal to 3H. Six equalising pulses spaced at H/2 seconds occur during each of these two intervals. These equalising pulses assure horizontal synchronisation and minimise interlace problems. Thus, the total width of the vertical sync pulse and the preceding and following series of equalisation pulses is 9H. This sequence is then followed by the reminder of the vertical blanking pulse, during which time the horizontal syncs continue to occur at their normal spacing. Table 2 shows the difference in vertical sync between NTSC and PAL.

Vertical sync	NTSC	NTSC (gen)	PAL	PAL (gen)
Blanking width	20H	20H	25H	25H
Num. equalising	6	6	5	5
Num. vert. sync	6	6	*5*	*5*
Equalising width ms	2.30	3.00	2.35	3.00
Vert. sync width ms	27.10	27.00	27.30	27.00

Table 2: The difference in vertical sync between NTSC and PAL.

Equalising pulses assure that there is a similar pulse pattern immediately before and after the field broad pulses for both even and odd field. This assists the field pulse detection circuitry so that the field scans are correctly interlaced. From Table 2, the equalising pulse width is 3 µseconds and the reset is 29 µseconds.

The vertical sync pulse is designed in the same way as the equalising pulse, only different in the time duration. From Table 2, the vertical sync width is 27 µseconds and the reset is 5 µseconds.

Complex video signal

The CVS consists of all the synchronisation information for the television. It is constructed by integrating a certain number of line and field sync signals together, taking into account the difference in the number of lines between NTSC and PAL. The difference between number of lines for both NTSC and PAL is listed in Table 3.

Complex video sync	NTSC (odd)	NTSC (even)	PAL (odd)	PAL (even)
num. of vert. syncs	6	6	5	5
num. of equal. pulses	6	5	5	4
num. of blanking lines	12	13	17	17
num. of display lines	240	240	288	288
num. of blanking lines	1	1	0	0
num. of half lines	1	0	0	1
num. of equal. pulses	6	6	5	*5*

Table 3: The designed parameters for NTSC and PAL complex sync signal.

Experimental results

For the prototype, the camera was built to NTSC format, with software compensating for the difference between that and PAL. Consequently, the image displayed in NTSC format was same as the 'original'. However, if the signal is displayed on a PAL format television, the video would be compressed vertically. This effect is due to the different vertical resolutions of NTSC and PAL video formats. Thus, some adjustments had to be made, so that the NTSC data could be display as PAL format. To obtain the original uncompressed signal, there were two methods - compressing the horizontal resolution or expanding the vertical resolution. Since the line period of a television is usually fixed, the horizontal resolution of the television can be adjusted by the sampling clock frequency. However, this requires another, faster, clock and some interface circuit. The other method is to expand the vertical resolution and it can be done in software with the existing hardware.

From Table 3, the ratio of the vertical resolution between NTSC and PAL systems is 5:6. Therefore, PAL video format requires an expansion 1/5 from the original NTSC video signal. The image is expanded through the line mapping method. The first 4 lines of the original image (NTSC) is directly mapped to the destination image (PAL), and the 5th line is mapped to the 5th and 6th of the destination (PAL) image. As a result, the destination image will be expanded by 1/5. The results is shown in Figure 4.

Fig 4. The image displayed in PAL format with expansion

Conclusions

The prototype camera worked, albeit with a very noisy picture, as it was built on a wirewrap board. The prototype showed that the basic concept was valid, especially as the total component cost was under US$50. Current work is to design an SMT based version. This will eliminate a lot of the noise problems. Also, many of the ttl interface and timing components have been replaced by two integrated circuits from TI. The component cost for this design is estimated to be around US$40. Elimination of the external memory, by using a microprocessor with internal memory is the next stage of development. This will reduce the cost even further. Finally, using EDA techniques, a fully integrated version, using just four main chips, is the final goal. This should then reach the US$20 cost that was the original aim.

Since the initial development of the camera was for toy and domestic uses, a number of other applications have arisen. In the field of machine vision, for example, expensive frame grabbers are used to take the composite video signal and convert it into a digital one. As the original signal coming from the ccd array is easily converted to a digital one by the use of just an ADC, most of this intervening circuitry is really unnecessary. A concurrent programme is investigating whether image processing techniques, such as Hough Transform edge detection, can be integrated into the camera so that only needed information goes to the computer, thus lowering the cost of such applications.

Similarly, another application is in the security area. As it is possible to selectively scan the image, resolution enhancement can be integrated into the software, thus providing an intelligent camera that can eliminate the need for expensive control equipment.

Acknowledgement

I would like to thank Mr Gary Wong Sing , who did the construction and programming of the prototype.